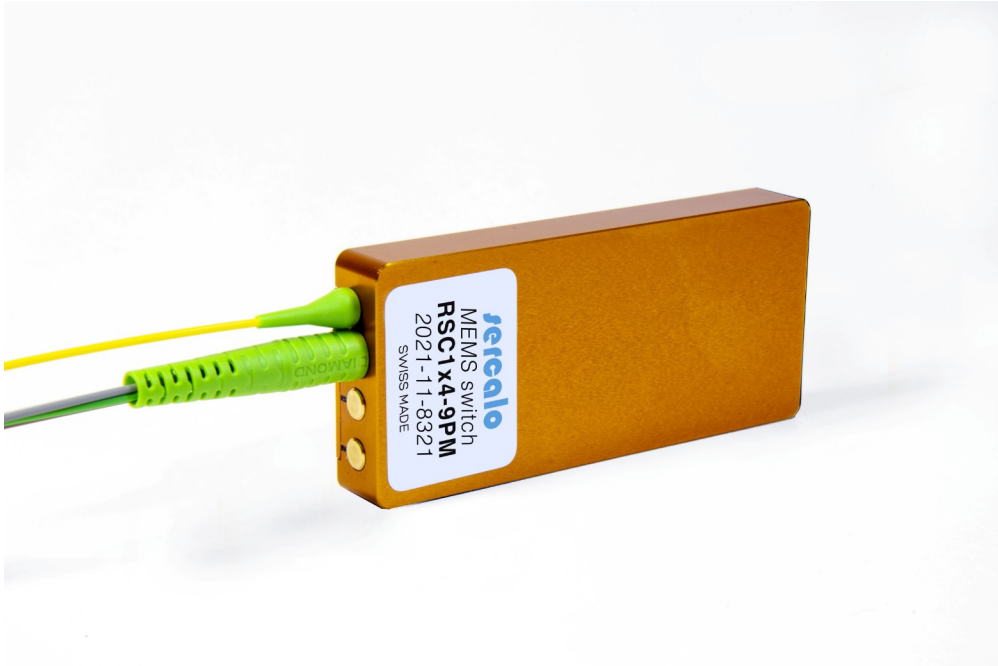
RSC

Coaxial Fiber Optic 1xN Switch with Interface



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1 In This Manual

This manual describes the optical, electrical and mechanical specifications of the rSC coaxial 1xN fiber optic switches. It additionally details the communication protocol required to operate the device.

2 Description

sercalo's rSC 1xN switch is an opto-mechanical fiber optic switch based on a coaxial design where a single MEMS mirror redirects light from a common fiber to one of N ports. The component is bidirectional, that is the common port can be used as input or output of the light signal.

The underlying MEMS technology permits obtaining low insertion loss combined with high crosstalk between channels with constant switching performance. The hermetically sealed MEMS and the laser welded fiber collimator guarantee broad temperature range and superior long term stability. No epoxy is present in the optical path. The miniature package withstands rugged environments and is well suited for direct mounting on printed circuit boards.

Depending on the model, the switch communicate over UART, I²C/SMBus and/or TTL/CMOS-compatible parallel interface (see Figure 1). Table 1 presents a comparison of the available interfaces and communication protocols on different switch families.

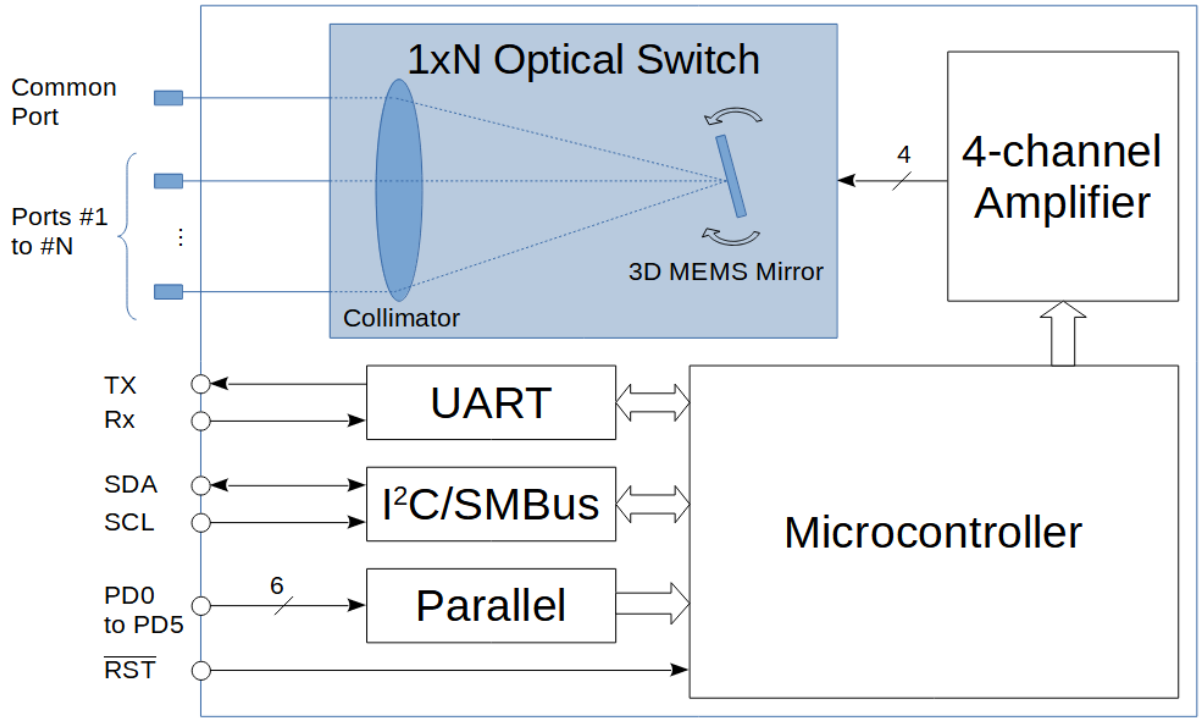

Figure 1 – Functional block diagram

Port count	Available interfaces		
	UART	*I²C/SMBus*	*Parallel*
up to 16 ports	yes	yes	yes
from 17 ports	yes	yes	partial

Table 1 – Available interfaces.

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3 Product Dimensions and Connector Pin Assignments

Figure 2 depicts the device layout. All dimensions are shown in millimeters.

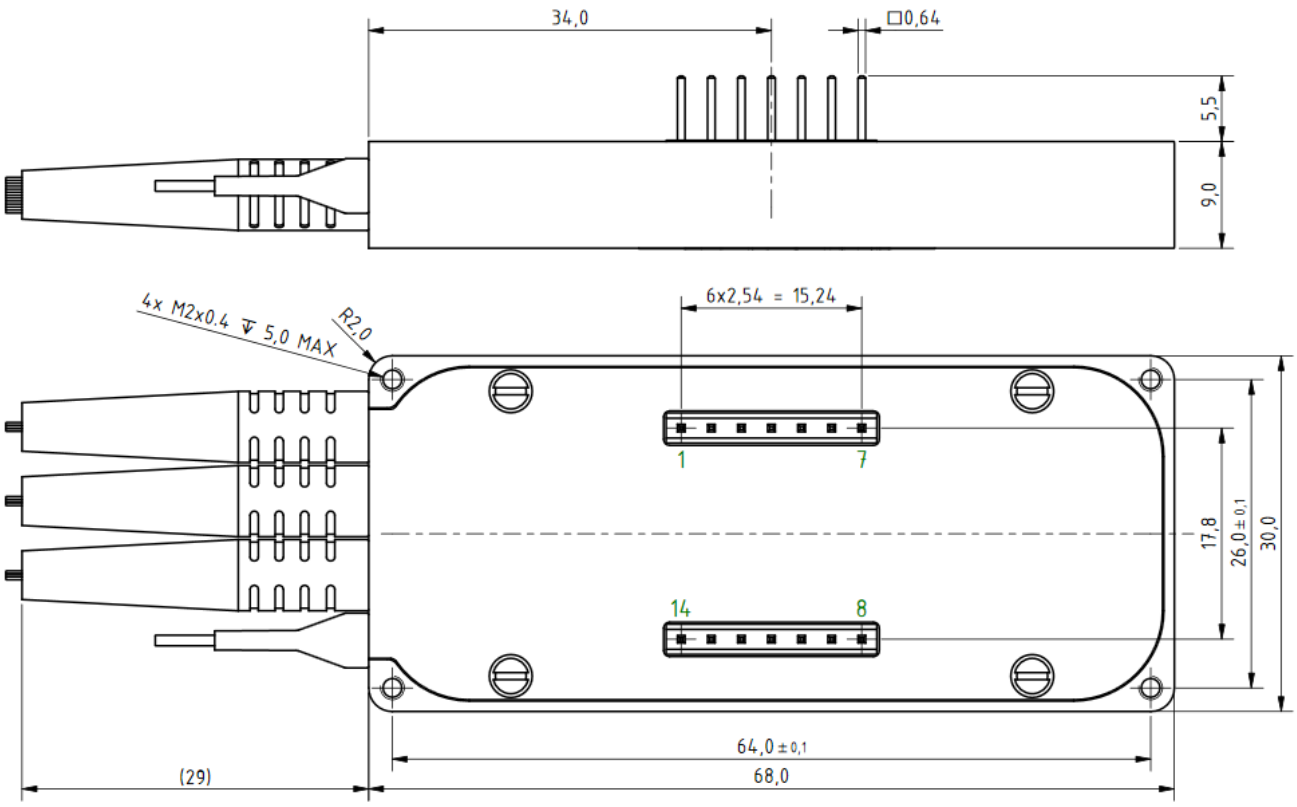

Figure 2 – Device dimensions

4 Connector Pin Assignments

The pin assignments for the connector is detailed in Tables 2.

Please note the following points:

- ➔ **UART TX** signal carries data *from* the product, while **UART RX** signal carries data *to* the product.
- ➔ The UART interface uses TTL/CMOS voltage levels. A voltage translator is required in order to communicate with the driver board using an RS-232 interface (see Section 8.2).
- ➔ The **Interface mode select** pins must be set either to 0 or 1 logic level *before* power on or reset and can not be changed during operation.
- ➔ When using SMBus/I²C interface, the **SMBus/I²C address** pins must be set either to 0 or 1 logic level *before* power on or reset and can not be changed during operation.
- ➔ **System reset**, **Parallel data**, **Parallel strobe**, **UART RX/TX**, **SMBus/I²C address** and **SMBus/I²C SDA/SCL** signals are connected to internal high impedance pull-up resistors. Unused pins can be let unconnected.
- ➔ Let reserved pins unconnected.

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Pin	Name	Description	Pin	Name	Description
1	IF1	Interface mode select 1, see Table 3	8	IF0	Interface mode select 0, see Table 3
2	VDD	Supply voltage	9	ADDR2 PD2	SMBus/I2C Address bit 2 Parallel Data bit 2
3	STROB E	Falling edge-triggered parallel strobe	10	$\overline{\text{DONE}}$	$\overline{\text{DONE}}$ asserts low to indicate that the switch is ready to accept new commands
4	GND	Ground	11	GND	Ground
5	ADDR0 PD0	SMBus/I2C Address bit 0 Parallel Data bit 0	12	ADDR1 PD1	SMBus/I2C Address bit 1 Parallel Data bit 1
6	SDA TX	SMBus/I^{2}C Serial Data UART TX	13	ADDR3 PD3	SMBus/I2C Address bit 3 Parallel Data bit 3
7	SCL RX	SMBus/I^{2}C Serial Clock UART RX	14	$\overline{\text{RST}}$	Active-low system reset

Table 2 – Connector pin assignment

IF1 pin	IF0 pin	*UART*	*I^{2}C/SMBus*	*Parallel*
0	0	disabled	enabled	disabled
0	1	disabled	disabled	enabled
1	0	enabled	disabled	disabled
1	1	disabled	disabled	enabled

Table 3 – Functionality of IF0 and IF1 pins.

5 Fiber Marking

1.1 Versions with tight-buffered 900um fibers

Individual ports of switches with tight-buffered 900um fibers are identified using a clip sleeve marker. In addition the common port has a yellow sleeve.

1.2 Versions with 250um bare fibers

Individual ports of switches with 250um bare fibers are identified using a color code.

1.2.1 1x4 switches

Ports are organized in single fibers marked as indicated on Table 4.

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Port	Fiber Color
Common	Yellow
1	Green
2	Brown
3	Blue
4	Transparent

Table 4 – Fiber colors for rSC1x4

1.2.2 1x8, 1x12 and 1x16 switches

Common port has a yellow sleeve. Other ports are marked as indicated on Table 5.

Port	Ribbon	Fiber Color rSC1x8	Fiber Color rSC1x12	Fiber Color rSC1x16
Common	NO	Yellow	Yellow	Yellow
1	A	Blue	Blue	Blue
2		Orange	Orange	Orange
3		Green	Green	Green
4		Brown	Brown	Brown
5		Grey	Grey	Grey
6		White	White	White
7		Red	Red	Red
8		Black	Black	Black
9	B		Blue	Blue
10			Orange	Orange
11			Green	Green
12			Brown	Brown
13				Grey
14				White
15				Red
16				Black

Table 5 – Fiber colors for rSC1x8, rSC1x12 and rSC1x16 (bare fiber colors). The color of the 900 um sleeve is identical for each bundle of 8.

1.2.3 1x24 and 1x36 switches

Common port has a yellow sleeve. Other ports are marked as indicated on Table 6.

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Port	Ribbon	Fiber Color rSC1x24	Fiber Color rSC1x36
Common	NO	Yellow	Yellow
1	A	Blue	Blue
2		Orange	Orange
3		Green	Green
4		Brown	Brown
5		Grey	Grey
6		White	White
7		Red	Red
8		Black	Black
9		Yellow	Yellow
10		Purple	Purple
11		Rose	Rose
12		Turquoise	Turquoise
13	B	Blue	Blue
14		Orange	Orange
15		Green	Green
16		Brown	Brown
17		Grey	Grey
18		White	White
19		Red	Red
20		Black	Black
21		Yellow	Yellow
22		Purple	Purple
23		Rose	Rose
24		Turquoise	Turquoise
25	C		Blue
26			Orange
27			Green
28			Brown
29			Grey
30			White
31			Red
32			Black
33			Yellow
34			Purple
35			Rose
36			Turquoise

Table 6 – Fiber colors (bare fiber only) for rSC1x24 and rSC1x36. The 900 um color is the same for each group of 12.

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6 Using the UART Interface

The device is equipped with a Universal Asynchronous Receiver-Transmitter (UART) with TTL/CMOS-compatible voltage levels. UART TX signal carries data *from* the product, while UART RX signal carries data *to* the product.

Table 7 lists the requirements for the UART settings. The default baud rate (after power on or reset) is 115200 baud. Baud rate remains in effect otherwise changed by the user.

Parameter	Factory setting
Transmission rate [bps]	115200
Data bits	8
Parity	none
Stop bits	1
Flow control	none

Table 7 – RS-232 settings after power-on or reset

6.1 Command syntax

A **write sequence** consists of the following binary bytes (see Figure 3):

- *WRITE FLAG* (2 bytes): fixed preamble 0xEF 0xEF.
- *LENGTH* (1 byte): the number of bytes from ADDRESS to CHECKSUM, ADDRESS and CHECKSUM included.
- *ADDRESS* (1 byte): reserved for future purposes, use 0xFF.
- *COMMAND* (1 byte): refer to Section 9 for a list of available command codes.
- *DATA* (variable length): refer to Section 9 for a detailed explanation.
- *CHECKSUM* (1 byte): it is the least significant byte of the sum WRITE_FLAG_0 + WRITE_FLAG_1 + LENGTH + ADDRESS + COMMAND + DATA.

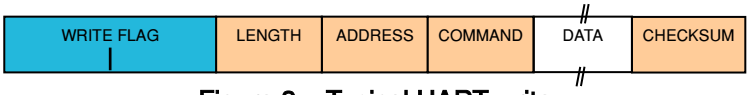

Figure 3 – Typical UART write

The device replies to each received command with a **reply sequence** consisting of the following binary bytes (see Figure 4):

- *REPLY FLAG* (2 bytes): fixed preamble 0xFE 0xFE.
- *LENGTH* (1 byte): the number of bytes from ADDRESS to CHECKSUM, ADDRESS and CHECKSUM included.
- *ADDRESS* (1 byte): reserved for future purposes, use 0xFF.
- *COMMAND* (1 byte): the same command code of the write sequence.
- *ERROR* (1 byte): refer to Section 11 for a list of error codes.
- *DATA* (variable length): refer to Section 9 for a detailed explanation.
- *CHECKSUM* (1 byte): it is the least significant byte of the sum REPLY_FLAG_0 + REPLY_FLAG_1 + LENGTH + ADDRESS + COMMAND + DATA.

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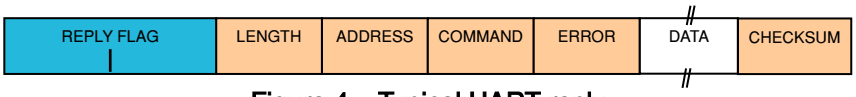

Figure 4 – Typical UART reply

6.2 Connect the UART interface to a PC

The UART interface can be directly connected to microcontrollers and any other electronic device with TTL/CMOS-compatible voltage levels, i.e. logic high ('1') is represented by V_{DD}, while a logic low ('0') is 0V. This is not the case for serial ports on personal computers whose voltage levels complies with the RS-232 standard. By the RS-232 standard a logic high ('1') is represented by a negative voltage (from -3V to -25V) while a logic low ('0') transmits a positive voltage (from +3V to +25V)[1].

One solution is to use the MAX232[2] integrated circuit or one of the many derivatives to convert signals from a RS-232 serial port to TTL signals. The other way is to use a USB-UART bridge based on CP2102 or FT232R integrated circuits which directly converts USB to UART. They are easily available on the market (some suppliers are listed on Table 8).

Supplier	Part Number
DigiKey	768-1017-ND
Mouser	895-TTL-232R-5V-PCB
eXtreme Electronics	SKU00201
Sparkfun	FTDI Basic Breakout - 5V
Adafruit	954

Table 8 – Example of USB-to-UART bridge suppliers

If a Windows-based PC and HyperTerminal are used, the suggested configuration is displayed in Figure 5.

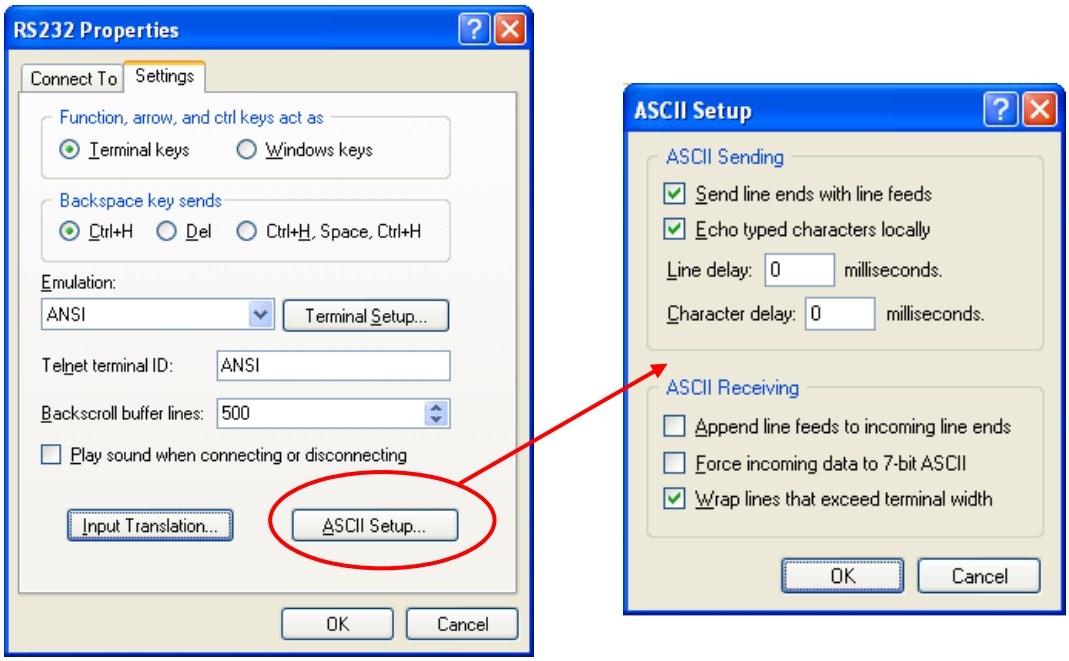

Figure 5 – HyperTerminal RS-232 properties and ASCII setup.

[1] https://en.wikipedia.org/wiki/RS-232#Voltage_levels

[2] https://en.wikipedia.org/wiki/MAX232

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7 Using the SMBus/I²C Interface

The device is equipped with an SMBus serial I/O peripheral that is compliant with both the System Management Bus Specification and the I²C-Bus Specification. SMBus is a trademark of Intel; I²C is a trademark of Phillips Semiconductor.

Each transmission is terminated with a Packet Error Code (PEC) byte, compliant to SMBus specification version 2.0 and 1.1. The byte is calculated over the entire message including the address and read/write bit (see Section 7.6 for details).

Please note that the device, after a successful write sequence, delay any further transmission by holding SCK low until the command is executed.

7.1 Device address

- The address of rSC 1x4, 1x8, 1x12 and 1x16 switches can be programmed using the dedicated ADDR0~ADDR3 pins when IF0 is tied to ground (see Table 9).

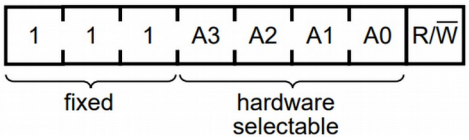
IF0 pin	ADDR pins				SMBus/I²C address
0	A3	A2	A1	A0	
1	-	-	-	-	SMBus/I²C disabled

Table 9 – SMBus/I2C address (mSC – miniature size)

7.2 Send commands to device

A write sequence consists of the following elements (see Figure 6):

1. A *start* condition: it consists of a falling edge on SDA while SCL is high.
2. The *address byte*, i.e. 7 bits corresponding to the device address and the R/W bit set as “write” (the R/W bit is set to logic 1 to indicate a “read” operation and cleared to logic 0 to indicate a “write” operation).
3. A *command code*: refer to Section 9 for a list of available command codes.
4. The *parameter(s) length*, i.e. the number *n* of bytes composing the following optional parameters. This field is mandatory: if no parameters are required, set it to 0x00.
5. The *optional parameters*: refer to Section 9 for a detailed explanation.
6. *CRC-8.*
7. A *stop* condition: it consists of a rising edge on SDA while SCL is high.

The device replies to each received byte with an “ACK” as a confirmation. An ACK consists of a low level on SDA sampled when SCL is high. If the ACK signal is not received, master must abort the transfer.

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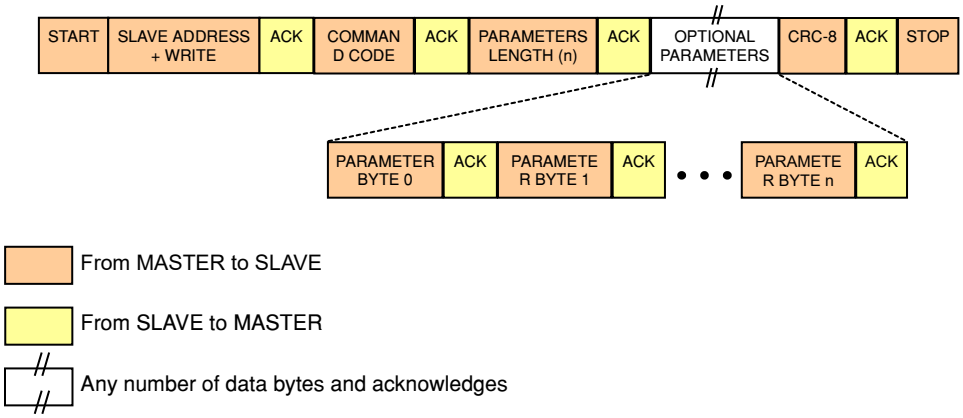

Figure 6 – Typical SMBus/I²C successful write (master to slave)

7.3 Receive data from device

After a successful transmission, as detailed in paragraph 7.2, device always has a reply that can be optionally read by master. A read sequence for a successfully executed command consists of the following elements (see Figure 7):

1. A *start* condition: it consists of a falling edge on SDA while SCL is high.
2. The *address byte*, i.e. 7 bits corresponding to the device address and the R/W bit set as “read” (the R/W bit is set to logic 1 to indicate a “read” operation and cleared to logic 0 to indicate a “write” operation).
3. A *command code*: it is the last executed command, which this reply refers.
4. The *parameter(s) length*, i.e. the number *n* of bytes composing the following optional parameters. If no parameters will follow, this field is set to 0x00.
5. The *optional parameters*: refer to Section 9 for a detailed explanation.
6. *CRC-8*.
7. A *stop* condition: it consists of a rising edge on SDA while SCL is high.

The master must replies to each received byte with an “ACK” as a confirmation. An ACK consists of a low level on SDA sampled when SCL is high. Only the last byte must be confirmed with a “NACK”. A NACK consists of a high level on SDA sampled when SCL is high.

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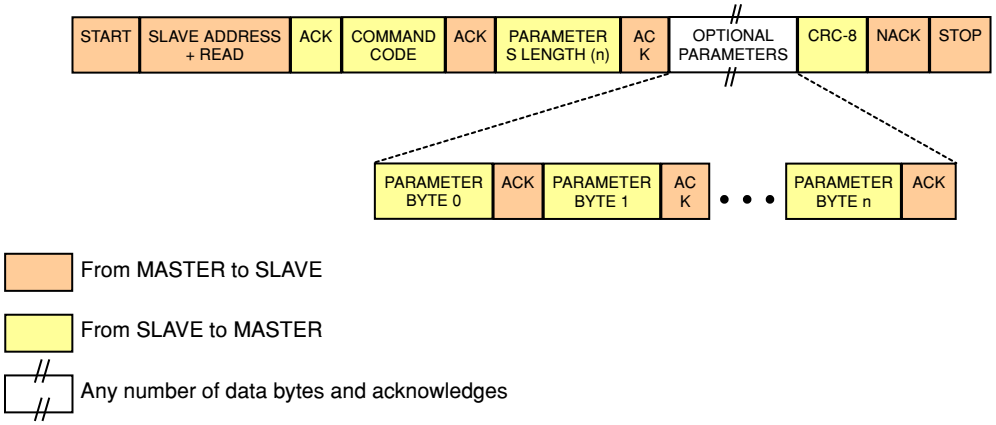

Figure 7 – Typical SMBus/I²C successful read (slave to master)

7.4 Receive an error from device

If the previous command returns an error, it can be optionally read and detect by the master. A read sequence for a command returning an error consists in the following elements:

1. A *start* condition: it consists of a falling edge on SDA while SCL is high.
2. The *address byte*, i.e. 7 bits corresponding to the device address and the R/W bit set as “read” (the R/W bit is set to logic 1 to indicate a “read” operation and cleared to logic 0 to indicate a “write” operation).
3. A *command code* plus the value 0x80.
4. The *error number*: see Section 11 for a list of error codes.
5. *CRC-8*.
6. A *stop* condition: it consists of a rising edge on SDA while SCL is high.

The master must replies to each received byte with an “ACK” as a confirmation. An ACK consists of a low level on SDA sampled when SCL is high. Only the last byte must be confirmed with a “NACK”. A NACK consists of a high level on SDA sampled when SCL is high.

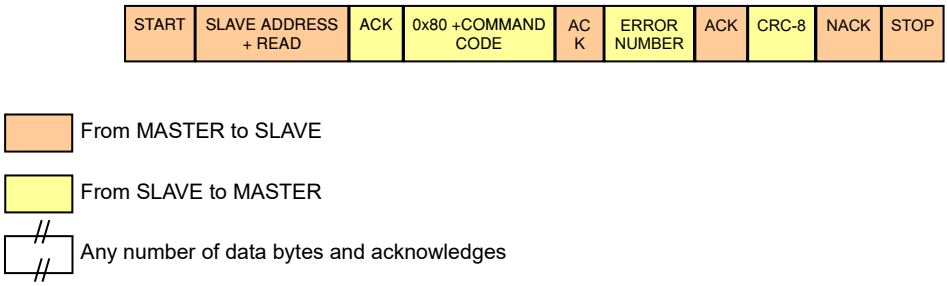

Figure 8 – Device returns an error (slave to master)

7.5 Hold master communication sequence

If the device is addressed during the execution of a command, it pulls down the SCL line in order to force the master into a wait state. By releasing the SCL line, the device indicates that internal processing is terminated and that transmission may be continued. The maximum duration for command execution can vary depending on the command.

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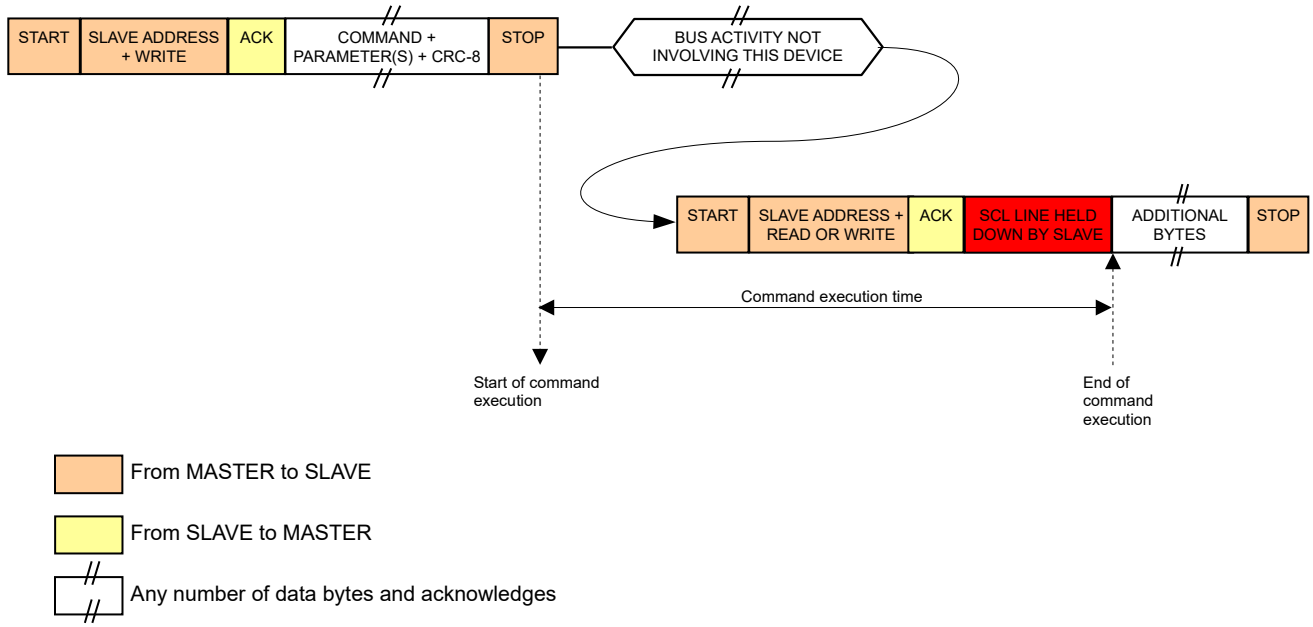

Figure 9 – Communication sequence with SCL line held down until command is executed

7.6 Example of CRC-8 generation

The SMBus/I²C uses a PEC (packet error code) compliant to SMBus specification version 1.1 and 2.0. The polynomial used is x^8+x^2+x+1 i.e. the CRC-8-ATM HEC algorithm, initialized to zero. An example of a C function that performs the calculation is presented below.

```
unsigned char crc8(unsigned char MsgLen, const unsigned char *Msg){
/* Lookup table for CRC codes
// CRC-8, poly = x^8 + x^2 + x^1 + x^0, init = 0 */

static unsigned char crc8_table[256] = {
   0x00, 0x07, 0x0E, 0x09, 0x1C, 0x1B, 0x12, 0x15, 0x38, 0x3F, 0x36, 0x31,
   0x24, 0x23, 0x2A, 0x2D, 0x70, 0x77, 0x7E, 0x79, 0x6C, 0x6B, 0x62, 0x65,
   0x48, 0x4F, 0x46, 0x41, 0x54, 0x53, 0x5A, 0x5D, 0xE0, 0xE7, 0xEE, 0xE9,
   0xFC, 0xFB, 0xF2, 0xF5, 0xD8, 0xDF, 0xD6, 0xD1, 0xC4, 0xC3, 0xCA, 0xCD,
   0x90, 0x97, 0x9E, 0x99, 0x8C, 0x8B, 0x82, 0x85, 0xA8, 0xAF, 0xA6, 0xA1,
   0xB4, 0xB3, 0xBA, 0xBD, 0xC7, 0xC0, 0xC9, 0xCE, 0xDB, 0xDC, 0xD5, 0xD2,
   0xFF, 0xF8, 0xF1, 0xF6, 0xE3, 0xE4, 0xED, 0xEA, 0xB7, 0xB0, 0xB9, 0xBE,
   0xAB, 0xAC, 0xA5, 0xA2, 0x8F, 0x88, 0x81, 0x86, 0x93, 0x94, 0x9D, 0x9A,
   0x27, 0x20, 0x29, 0x2E, 0x3B, 0x3C, 0x35, 0x32, 0x1F, 0x18, 0x11, 0x16,
   0x03, 0x04, 0x0D, 0x0A, 0x57, 0x50, 0x59, 0x5E, 0x4B, 0x4C, 0x45, 0x42,
   0x6F, 0x68, 0x61, 0x66, 0x73, 0x74, 0x7D, 0x7A, 0x89, 0x8E, 0x87, 0x80,
   0x95, 0x92, 0x9B, 0x9C, 0xB1, 0xB6, 0xBF, 0xB8, 0xAD, 0xAA, 0xA3, 0xA4,
   0xF9, 0xFE, 0xF7, 0xF0, 0xE5, 0xE2, 0xEB, 0xEC, 0xC1, 0xC6, 0xCF, 0xC8,
   0xDD, 0xDA, 0xD3, 0xD4, 0x69, 0x6E, 0x67, 0x60, 0x75, 0x72, 0x7B, 0x7C,
   0x51, 0x56, 0x5F, 0x58, 0x4D, 0x4A, 0x43, 0x44, 0x19, 0x1E, 0x17, 0x10,
   0x05, 0x02, 0x0B, 0x0C, 0x21, 0x26, 0x2F, 0x28, 0x3D, 0x3A, 0x33, 0x34,
   0x4E, 0x49, 0x40, 0x47, 0x52, 0x55, 0x5C, 0x5B, 0x76, 0x71, 0x78, 0x7F,
   0x6A, 0x6D, 0x64, 0x63, 0x3E, 0x39, 0x30, 0x37, 0x22, 0x25, 0x2C, 0x2B,
   0x06, 0x01, 0x08, 0x0F, 0x1A, 0x1D, 0x14, 0x13, 0xAE, 0xA9, 0xA0, 0xA7,
   0xB2, 0xB5, 0xBC, 0xBB, 0x96, 0x91, 0x98, 0x9F, 0x8A, 0x8D, 0x84, 0x83,
   0xDE, 0xD9, 0xD0, 0xD7, 0xC2, 0xC5, 0xCC, 0xCB, 0xE6, 0xE1, 0xE8, 0xEF,
   0xFA, 0xFD, 0xF4, 0xF3 };

register unsigned char crcVal = 0x00;
```

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```
while (MsgLen-- > 0)
   crcVal = crc8_table[crcVal ^ *Msg++];

return crcVal;
}
```

8 Using the TTL/CMOS Parallel Interface

The switch can be controlled with a TTL/CMOS-compatible parallel interface. If the parallel interface is not used, unconnected STROBE and PD0-PD3 pins are kept to logic high ('1') through internal pull-up resistors. Only the first 16 ports can be addressed through parallel interface. Data is captured by the STROBE control pin during any high-to-low transition (see Figure 10).

The optical state is defined by data lines PD0-PD3 accordingly to Tables 11 and 12.

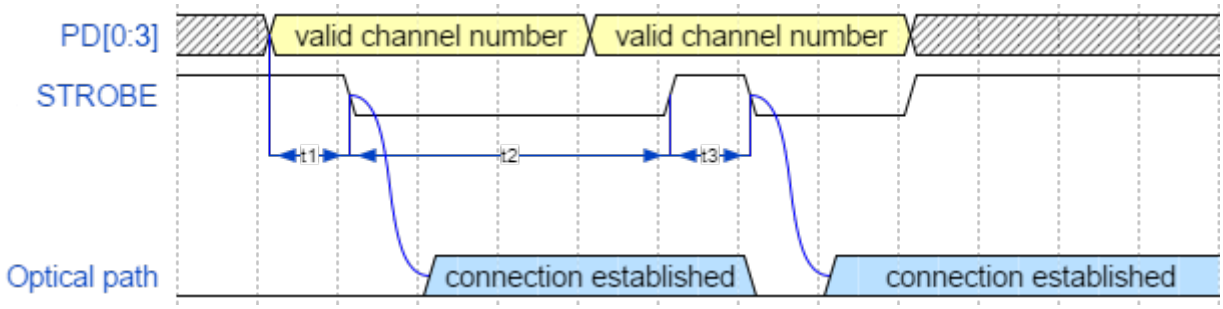

Figure 10 – Typical timing diagram

Parameter[3]	Limit	Description
t_1	1 µs min	PD[0:3] setup time
t_2	2 µs min	STROBE pulse width
t_3	5 µs min	STROBE hold time

Table 10 – Timing specifications for parallel interface

[3]Rise and fall times should be no longer than 1 µs.

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Switch type	Port	PD 0	PD 1	PD 2	PD 3
1x4	None	1	1	1	X
	1	0	0	0	X
	2	1	0	0	X
	3	0	1	0	X
	4	1	1	0	X
1x8	None	1	1	1	1
	1	0	0	0	0
	2	1	0	0	0
	3	0	1	0	0
	4	1	1	0	0
	5	0	0	1	0
	6	1	0	1	0
	7	0	1	1	0
	8	1	1	1	0
1x16	None	Not addressable			
	1	0	0	0	0
	2	1	0	0	0
	3	0	1	0	0
	4	1	1	0	0
	5	0	0	1	0
	6	1	0	1	0
	7	0	1	1	0
	8	1	1	1	0
	9	0	0	0	1
	10	1	0	0	1
	11	0	1	0	1
	12	1	1	0	1
	13	0	0	1	1
	14	1	0	1	1
	15	0	1	1	1
	16	1	1	1	1

Switch type	Port	PD 0	PD 1	PD 2	PD 3
1x24	None	Not addressable			
	1	0	0	0	0
	2	1	0	0	0
	3	0	1	0	0
	4	1	1	0	0
	5	0	0	1	0
	6	1	0	1	0
	7	0	1	1	0
	8	1	1	1	0
	9	0	0	0	1
	10	1	0	0	1
	11	0	1	0	1
	12	1	1	0	1
	13	0	0	1	1
	14	1	0	1	1
	15	0	1	1	1
	16	1	1	1	1
	17	Not addressable			
	18				
	19				
	20				
	21				
	22				
	23				
	24				

Table 11 – Port selection truth table for rSC1x4, rSC1x8, rSC1x16 and rSC1x24

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Switch type	Port	PD 0	PD 1	PD 2	PD 3
1x36	None	Not addressable			
	1	0	0	0	0
	2	1	0	0	0
	3	0	1	0	0
	4	1	1	0	0
	5	0	0	1	0
	6	1	0	1	0
	7	0	1	1	0
	8	1	1	1	0
	9	0	0	0	1
	10	1	0	0	1
	11	0	1	0	1
	12	1	1	0	1
	13	0	0	1	1
	14	1	0	1	1
	15	0	1	1	1
	16	1	1	1	1
	17	Not addressable			
	18				
	19				
	20				
	21				
	22				
	23				
	24				
	25				
	26				
	27				
	28				
	29				
	30				
	31				
	32				
	33				
	34				
	35				
	36				

Table 12 – Port selection truth table for rSC1x36

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9 Command Reference

The available commands are listed in Table 13 and detailed in the following subsections.

Binary	Description
0x01	Product information
0x02	Get channel
0x03	Reset
0x04	Set channel

Table 13 – List of available commands

9.1 Product information

Returns the system identification.

- Write sequence:

0xEF	0xEF	0x03	0xFF	0x01	0xE1

- Response:

0xFE	0xFE	0x2C	0xFF	0x01	error

vendor code	switch type	hardware version	firmware version	production date	serial number	checksum

Item	Length	Coding	Notes
Vendor code	10	ASCII	Unused bytes are filled with ‘;’
Switch type	10	ASCII	Unused bytes are filled with ‘;’
Hardware version	2	binary	<0: mayor_revision>.<1: minor_revision>
Firmware version	2	binary	<0: mayor_revision>.<1: minor_revision>
Production date	4	binary	YYYY-MM-DD
Serial number	8	ASCII	Unused bytes are filled with ‘;’

9.2 Get channel

Returns the current optical switch network configuration.

- Write sequence:

0xEF	0xEF	0x03	0xFF	0x02	0xE2

- Response:

0xFE	0xFE	0x05	0xFF	0x02	error	channel	checksum

9.3 Reset

Resets the system.

- Write sequence:

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0xEF | 0xEF	0x03	0xFF	0x03	0xE3	

- Response:

0xFE | 0xFE	0x04	0xFF	0x03	error	checksum

9.4 Set channel

Sets the optical switch network.

- Write sequence:

0xEF | 0xEF	0x04	0xFF	0x04	channel	checksum

- Response:

0xFE | 0xFE	0x04	0xFF	0x04	error	checksum

Table 14 contains a comprehensive list of write sequences.

Channel number	Write sequence	Channel number	Write sequence
0	0x EF EF 04 FF 04 00 E5	19	0x EF EF 04 FF 04 13 F8
1	0x EF EF 04 FF 04 01 E6	20	0x EF EF 04 FF 04 14 F9
2	0x EF EF 04 FF 04 02 E7	21	0x EF EF 04 FF 04 15 FA
3	0x EF EF 04 FF 04 03 E8	22	0x EF EF 04 FF 04 16 FB
4	0x EF EF 04 FF 04 04 E9	23	0x EF EF 04 FF 04 17 FC
5	0x EF EF 04 FF 04 05 EA	24	0x EF EF 04 FF 04 18 FD
6	0x EF EF 04 FF 04 06 EB	25	0x EF EF 04 FF 04 19 FE
7	0x EF EF 04 FF 04 07 EC	26	0x EF EF 04 FF 04 1A FF
8	0x EF EF 04 FF 04 08 ED	27	0x EF EF 04 FF 04 1B 00
9	0x EF EF 04 FF 04 09 EE	28	0x EF EF 04 FF 04 1C 01
10	0x EF EF 04 FF 04 0A EF	29	0x EF EF 04 FF 04 1D 02
11	0x EF EF 04 FF 04 0B F0	30	0x EF EF 04 FF 04 1E 03
12	0x EF EF 04 FF 04 0C F1	31	0x EF EF 04 FF 04 1F 04
13	0x EF EF 04 FF 04 0D F2	32	0x EF EF 04 FF 04 20 05
14	0x EF EF 04 FF 04 0E F3	33	0x EF EF 04 FF 04 21 06
15	0x EF EF 04 FF 04 0F F4	34	0x EF EF 04 FF 04 22 07
16	0x EF EF 04 FF 04 10 F5	35	0x EF EF 04 FF 04 23 08
17	0x EF EF 04 FF 04 11 F6	36	0x EF EF 04 FF 04 24 09
18	0x EF EF 04 FF 04 12 F7		

Table 14 – List of write sequences for setting a specific channel number

10 System Reset

A system reset is performed:

- By asserting the system reset ($\overline{RST}$) signal (see Table 2)
- By using the reset command (see Paragraph 9.3)
- After any powering on

The reset brings the switch to its initial state:

- The optical path is set to zero (the common port is not connected to any of the other ports)
- The receive and transmit buffers of the UART and SMBus/I^{2}C interfaces are flushed and any pending error is cleared

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11 Error Codes

The following table gives information about error codes.

Error number	Description
0	No error
1	Command unknown
2	Invalid parameter(s)
3	Command fail
4	Checksum error

Table 15 – List of error codes

12 Absolute Maximum Ratings

Applicable absolute maximum ratings for the full operating temperature range without causing irreversible damage to the device are listed in Table 16.

	Unit	Min	Max
Operation temperature	˚C	-5	70
Storage temperature	˚C	-40	85
Maximum optical power	mW		500
Voltage on V_{DD}	V	GND-0.2	5.5
Voltage on any IO pin	V	GND-0.2	5.8
Total current sunk into V_{DD}	mA		300
Current sourced or sunk by any IO pin	mA	-100	100

Table 16 – Absolute maximum ratings

13 Optical Specifications

Please refer to the datasheet for the optical specifications.

14 Electrical Specifications

	Unit	Min	Typ	Max
Supply voltage	V	4.75	5	5.25
Power consumption, normal mode	mW			150
Power consumption, standby mode	mW		40	
UART speed	baud	9600		115200
SMBus/I^2C bus speed	kbps	100		400
Input logic level low	V		0	0.6
Input logic level high	V	2.4	5	
Output logic level low	V		0	0.6
Output logic level high	V	2.6	3.3	
Reset inactive voltage[4]	V	2.4	5	
Reset active voltage	V		0	0.9
Reset pulse duration	µs	15		
Onboard pull-up resistor value	kΩ	110	165	330
Onboard pull-up voltage	V		3.3	

[4] Through onboard pull-up resistor.

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15 Package Specifications

	Unit	Min	Typ	Max
Pigtail length	cm	50		100
Body material		6061 aluminium alloy		
ROHS Compliance		2015/863/EU (no exceptions)		

16 Revision History

Version	Date	Modified	Approved	Changes
1.3	11.03.2020	P. Baroni	C. Marxer	Added Paragraph 10: system reset Added Table 14
1.4	07.04.2020	P. Baroni	C. Marxer	Removed color code information
1.5	16.04.2020	P. Baroni	C. Marxer	Table 2 and Errore: sorgente del riferimento non trovata: added signals description Paragraph 6: added additional details about UART
1.6	27.04.2020	P. Baroni	C. Marxer	Re-introduced color code information
1.7	13.05.2020	P. Baroni	C. Marxer	Paragraph 17: added option for LC-APC connector Paragraph 17: corrected wrong example for pigtail length Paragraph 1.1: added marking information for tight-buffer fibers
1.8	18.05.2020	P. Baroni	C. Marxer	Minor corrections
1.9	03.08.2020	P. Baroni	C. Marxer	Paragraph 8: corrected typo Paragraph 15: corrected pigtail length, updated RoHS compliance
1.10	03.12.2020	P. Baroni	C. Marxer	All RSC types in the same housing. New fiber boot.
1.11	16.02.2020	P. Baroni	C. Marxer	New functional block diagram Behaviour of parallel port if port count is greater than 16 Minor typos
1.12	2.03.2021	P. Baroni	C. Marxer	New front page picture

17 Ordering Information

rSC	1x16	-	9	R	-	05	FP

Switch type
rSC

Ports
1x4
1x8
1x12
1x16
1x24
1x32
1x36

Fiber type
9 = SMF28ULTRA
7 = SM980 for 1050nm
4 = SM400 for 630nm
Other fiber types and wavelengths upon request

Fiber sleeve type
B = 250um bare fibers
R = 8-fibers or 12-fibers ribbon
N = 900 µm sleeve

Pigtail length
Expressed in decimeters e.g.:
05 = 50 cm
10 = 100 cm

Connectors type
none = no connectors
FP = FC-PC
FA = FC-APC narrow key
LP = LC-PC
LA = LC-APC
SP = SC-PC
SA = SC-APC

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